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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/598,434	06/22/2000	Charles Robert Moore	AT9-99-451	5583

7590 05/24/2004

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EXAMINER	
CHANG, JUNGWON	
ART UNIT	**PAPER NUMBER**
2154	10

DATE MAILED: 05/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/598,434	MOORE, CHARLES ROBERT	
	Examiner	Art Unit	
	Jungwon Chang	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 and 2 have been canceled; claims 5, 7, 8, 12, 15, 16 and 20-22 have been amended. Claims 3-23 are presented for examination.

2. In response to obviousness-type double patenting rejection in the prior Office action dated 10/6/2003, Applicant offers to submit a terminal disclaimer to obviate double patenting rejection in the event that the copending U.S. Patent Application Serial No. 09/598,435 issues.

3. The text of those sections of Title 35, U.S. Code not included in this office action can be found in a prior office action.

4. Claims 3-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glew et al. (US 5,913,048), hereinafter Glew, in view of Webb, Jr. et al, hereinafter Webb.

5. As to claims 3 and 18, Glew discloses the invention substantially as claimed, including a processor (100, fig. 1; col. 3, lines 45-49), comprising:

a register set (150, fig. 1; col. 4, lines 16-23);

at least one execution unit (118, fig. 1) that executes load instructions to transfer data into said register set (col. 4, lines 35-40; col. 5, lines 22-45);

a load queue containing at least one entry, wherein said entry stores load data retrieved by a first load instruction (136, fig. 5; col. 11, lines 1-17); and

queue management logic that, responsive to execution of a second load instruction, detects by reference to said load queue whether a data hazard exist (i.e., out of order; col. 6, lines 48-56).

6. Glew does not specifically disclose outputs said load data retrieved by said first load instruction from said entry to said register set in accordance with said second load instruction. However, Webb discloses outputs said load data retrieved by said first load instruction from said entry to said register set in accordance with said second load instruction (col. 1, line 66 – col. 2, line 15; col. 4, lines 43-48; col. 7, lines 61-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Glew and Webb because Webb's bypass mechanism would improve program efficiency by reducing the false dependencies and instruction stalls.

7. As to claim 10, it is rejected for the same reasons set forth in claim 3 above. In addition, Glew discloses an interconnect fabric (158, fig. 1); a memory coupled to said interconnected fabric (175, fig. 1).

8. As to claims 4, 5, 11, 12, 19 and 20, Glew further discloses the entry stores a target address of said first load instruction (LDST of 136, fig. 5) and has a hazard flag

indicative of a possible data hazard (V of 136, fig. 5, col. 11, lines 10-17).

9. As to claims 6 and 14, Glew discloses register set comprising a general purpose register set (150, fig. 1; col. 4, lines 16-23).

10. As to claims 7 and 15, Glew discloses the queue management logic outputs said load data to a register in said

11. As to claims 8, 16 and 22, Glew discloses the queue management logic, responsive to detection of a data hazard, initiates re-execution of at least said first load instruction (col. 6, lines 62-65).

12. As to claims 9, 17 and 23, Glew discloses the queue management logic allocates a respective entry within said load queue to each load instruction upon dispatch and upon completion of said each load instruction, deallocates said respective entry (fig. 4; col. 9, line 48 – col. 10, line 5).

13. As to claim 13, Glew discloses a register set (150, fig. 1; col. 4, lines 16-23); at least one execution unit (118, fig. 1) that executes load instructions to transfer data into said register set (col. 4, lines 35-40; col. 5, lines 22-45); load queue comprises a first processor and the data processing system includes a second processor (col. 2, lines 40-44).

14. As to claim 21, it is rejected for the same reasons set forth in claims 1-3 and 18 above.

15. Applicant's arguments filed 2/4/2004 have been fully considered but they are not persuasive.

16. In the remarks, applicant argued in substance that

(1) Applicant offers to submit a terminal disclaimer to obviate the double patenting rejection in the event that the copending application issues.

(2) Glew and Webb do not teach or suggest, queue management logic that, responsive to execution of a second load instruction, detects by reference to said load queue whether a data hazard exists, and if so, outputs said load data retrieved by said first load instruction from said entry to said register set in accordance with said second load instruction".

(3) Glew does not teach or suggest the claimed "queue management logic." Indeed, Glew explicitly teaches at col. 6, lines 63-65 that a data hazard occasioned by a remote processor writing a speculatively read location causes "the load and subsequent operation clearly and re-executed to retrieve the correct data." Thus, Glew not only fails to disclose the claimed "queue management logic," but also explicitly teaches against Applicant's claimed technique of utilizing "load data retrieved by said first load instruction" and buffered within a load queue to satisfy the transfer of data into a register set indicated by a second load instruction.

(4) Webb teaches the use of store data from a store queue to satisfy a load operation indicated by a load instruction. Claim 1, in contrast, recites the use of load data within a load queue retrieved by a first load instruction.

17. Examiner respectfully traverses applicant's remarks.

As to point (1), the copending U.S. Patent Application Serial No. 09/598,435 has been issued, now U.S. patent No. 6,725,358 issued on 4/20/2004. Thus, applicant needs to file a terminal disclaimer.

As to points (2)-(4), Glew discloses load data retrieved by said first load instruction and buffered within a load queue to satisfy the transfer of data into a register set indicated by a second load instruction (i.e., reorder the out-of-order instruction (i.e., data hazard exists when the second load instruction is executed prior to the first load instruction) by storing load data retrieved by the first load instruction into the register according to the program order; col. 3, lines 32-42; col. 4, lines 35-40). Furthermore, Webb discloses load data retrieved by a first load instruction into register (col. 4, lines 34-48).

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jungwon Chang whose telephone number is (703)305-9669. The examiner can normally be reached on 9:30-6:00 (Monday-Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (703)308-9052. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-9669.

Jungwon Chang
May 14, 2004

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100